HARRIS

CDP65C51
CDP65C51A

CMOS Asynchronous Communications Interface Adapter (ACIA)

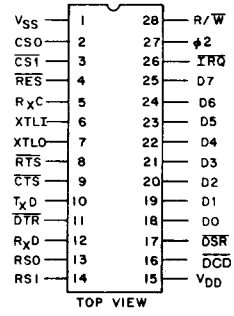
January 1991

Features

- Compatible With 8-Bit Microprocessors
- Full Duplex Operation With Buffered Receiver and Transmitter
- Data Set/Modem Control Functions
- Internal Baud Rate Generator With 15 Programmable Baud Rates (50 to 19,200)
- Program Selectable Internally or Externally Controlled Receiver Rate
- Operates at Baud Rates Up To 250,000 Via Proper Crystal or Clock Selection
- Programmable Word Lengths, Number of Stop Bits and Parity Bit Generation and Detection
- Programmable Interrupt Control
- Program Reset
- Program Selectable Serial Echo Mode
- Two Chip Selects
- 4MHz, 2MHz or 1MHz Operation (CDP65C51 and CDP65C51A-4, -2, -1 Types, Respectively)
- Single 3V to 6V Power Supply
- Full TTL Compatibility
- Synchronous $\overline{CTS}$ Operation

Pinout

PACKAGE TYPES D, E AND M
TOP VIEW



Description

The CDP65C51 and CDP65C51A Asynchronous Communications Interface Adapters (ACIA) provide an easily implemented, program controlled interface between 8-bit microprocessor based systems and serial communication data sets and modems. The CDP65C51A is identical to the CDP65C51 except for the implementation of the $\overline{CTS}$ function. If a not-clear-to-send signal is received during the transmission of a character, the CDP65C51A will first allow completion of that transmission, and then disable the transmitter.

The CDP65C51 and CDP65C51A have an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 19,200 baud, or 1/16 times an external clock rate. The receiver baud rate may be selected under program control to be either the transmitter rate, or at 1/16 times an external clock rate. The CDP65C51 and CDP65C51A have programmable word lengths of 5, 6, 7 or 8 bits; even, odd or no parity; 1, 1½ or 2 stop bits.

The CDP65C51 and CDP65C51A are designed for maximum programmed control from the CPU, to simplify hardware implementation. Three separate registers permit the CPU to easily select the CDP65C51A operating modes and data-checking parameters and determine operational status.

The **Command Register** controls parity, reciever echo mode, transmitter interrupt control, the state of the $\overline{RTS}$ line, receiver interrupt control, and the state of the $\overline{DTR}$ line.

The **Control Register** controls the number of stop bits, word length, receiver clock source and baud rate.

The **Status Register** indicates the states of the $\overline{IRQ}$, $\overline{DSR}$ and $\overline{DCD}$ lines, transmitter and receiver data registers, and overrun, framing and parity error conditions.

The transmitter and receiver data registers are used for temporary data storage by the CDP65C51A transmit and receive circuits.

The CDP65C51 and CDP65C51A-1, -2 and -4 types are capable of interfacing with microprocessors with cycle times of 1MHz, 2MHz and 4MHz, respectively.

The CDP65C51 and CDP65C51A are supplied in 28 lead hermetic dual-in-line sidebrazed ceramic packages (D suffix), in 28 lead dual-in-line plastic packages (E suffix) and in 28 lead dual-in-line small outline (SO) packages (M) suffix.

5
8-BIT BUS PERIPHERALS

File Number **2747**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +85°C (PACKAGE TYPE M)* ..... 425 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D ..... -55 to +125°C
PACKAGE TYPE E and M ..... -40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

RECOMMENDED OPERATING CONDITIONS at T_A = -40° to +85°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Operating Voltage Range	3	6	V
Input Voltage Range	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40° to +85°C, V_{DD} = 5V ± 5%

CHARACTERISTIC		LIMITS			UNITS
		Min.	Typ.	Max.	
Quiescent Device Current	I_{DD}	—	50	200	μA
Output Low Current (Sinking): V_{OL} = 0.4 V (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	I_{OL}	1.6	—	—	mA
Output High Current (Sourcing): V_{OH} = 4.6 V (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	I_{OH}	-1.6	—	—	mA
Output Low Voltage: I_{LOAD} = 1.6 mA (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	V_{OL}	—	—	0.4	V
Output High Voltage: I_{LOAD} = -1.6 mA (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	V_{OH}	4.6	—	—	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Input High Voltage (Except XTLI and XTLO) (XTLI and XTLO)	V_{IH}	 2 3	 — —	 V_{DD} V_{DD}	V
Input Leakage Current: V_{IN} = 0 to 5 V (ϕ2, R/$\overline{W}$, $\overline{RES}$, CS0, $\overline{CS1}$, RS0, RS1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$)	I_{IN}	—	—	±1	μA
Input Leakage Current for High Impedance State (D0-D7)	I_{TSI}	—	—	±1.2	μA
Output Leakage Current (off state): V_{OUT} = 5 V ($\overline{IRQ}$)	I_{OFF}	—	—	2	μA
Input Capacitance (except XTLI and XTLO)	C_{IN}	—	—	10	pF
Output Capacitance	C_{OUT}	—	—	10	pF

CDP65C51/51A INTERFACE REQUIREMENTS

This is a description of the interface requirements for the CDP65C51 and CDP65C51A. Fig. 1 is the Interface Diagram and the Terminal Diagram shows the pinout configuration for the CDP65C51A.

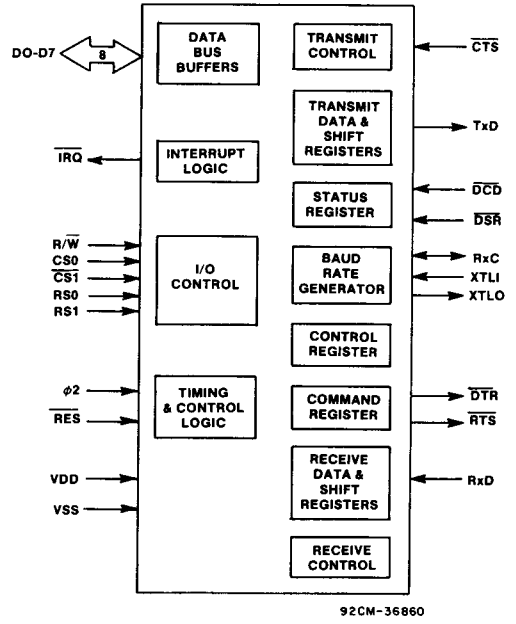


Fig. 1 - CDP65C51/51A interface diagram

MICROPROCESSOR INTERFACE SIGNAL DESCRIPTION

RES (Reset) (4)

During system initialization a low on the RES input will cause a hardware reset to occur. The Command Register and the Control Register will be cleared. The Status Register will be cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the DSR and DCD lines, and the transmitter Empty bit, which will be set. A hardware reset is required after power-up.

φ2 (Input Clock) (27)

The input clock is the system φ2 clock and is used to clock all data transfers between the system microprocessor and the CDP65C51/51A.

R/W (Read/Write) (28)

The R/W input, generated by the microprocessor, is used to control the direction of data transfers. A high on the R/W pin allows the processor to read the data supplied by the CDP65C51/51A, a low allows a write to the CDP65C51/51A.

IRQ (Interrupt Request) (26)

The IRQ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common IRQ microprocessor input. Normally at high level, IRQ goes low when an interrupt occurs.

D0-D7 (Data Bus) (18-25)

The D0-D7 pins are the eight data lines used to transfer data between the processor and the CDP65C51/51A. These lines are bidirectional and are normally high impedance except during Read cycles when the CDP65C51/51A are selected.

CS0, CS1 (Chip Selects) (2, 3)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The CDP65C51/51A are selected when CS0 is high and CS1 is low.

RS0, RS1 (Register Selects) (13, 14)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various CDP65C51/51A internal registers. The following table shows the internal register select coding.

TABLE I

RS1	RS0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command Register and bit 2 in the Status Register. The Control Register is unchanged by a Programmed Reset. It should be noted that the Programmed Reset is slightly different from the Hardware Reset (RES); these differences are shown in Figs. 3, 4 and 5.

ACIA/MODEM INTERFACE SIGNAL DESCRIPTION

XTLI, XTLO (Crystal Pins) (6, 7)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates (see "Generation of Non-Standard Baud Rates"). Alternatively, an externally generated clock may be used to drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

TxD (Transmit Data) (10)

The TxD output line is used to transfer serial NRZ (nonreturn-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or under control of an external clock. This selection is made by programming the Control Register.

RxD (Receive Data) (12)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or under the control of an externally generated receiver clock. The selection is made by programming the Control Register.

CDP65C51/51A INTERFACE REQUIREMENTS (Cont'd)

RxC (Receive Clock) (5)

The RxC is a bidirectional pin which serves as either the receiver 16X clock input or the receiver 16X clock output. The latter mode results if the internal baud-rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send) (8)

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send) (9)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

$\overline{DTR}$ (Data Terminal Ready) (11)

This output pin is used to indicate the status of the CDP65C51/51A to the modem. A low on $\overline{DTR}$ indicates the CDP65C51/51A is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready) (17)

The DSR Input pin is used to indicate to the CDP65C51/51A the status of the modem. A low indicates the "ready" state and a high, "not ready".

$\overline{DCD}$ (Data Carrier Detect) (16)

The $\overline{DCD}$ input pin is used to indicate to the CDP65C51/51A the status of the carrier detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

CDP65C51 AND CDP65C51A INTERNAL ORGANIZATION

This is a functional description of the CDP65C51/51A. A block diagram of the CDP65C51/51A is presented in Fig. 2.

DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bi-directional. When the R/$\overline{W}$ line is high an the chip is selected, the Data Bus Buffer passes the Data to the system data lines from the CDP65C51/51A internal data bus. When the R/$\overline{W}$ line is low and the chip is selected, the Data Bus Buffer writes the data from the system data bus to the internal data bus.

INTERRUPT LOGIC

The Interrupt Logic will cause the $\overline{IRQ}$ line to the microprocessor to go low when conditions are met that can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register if enabled. Bits 5 and 6 correspond to the Data Carrier Detect ($\overline{DCD}$) logic and the Data Set Ready ($\overline{DSR}$) logic. Bits 3 and 4 correspond to the Receiver Data Register full and the Transmitter Data Register empty conditions. These conditions can cause an interrupt request if enabled by the Command Register.

I/O CONTROL

The I/O Control Logic controls the selection of internal registers in preparation for a data transfer on the internal data bus and the direction of the transfer to or from the register.

The registers are selected by the Register Select and Chip Select and Read/Write lines as described in Table I, previously.

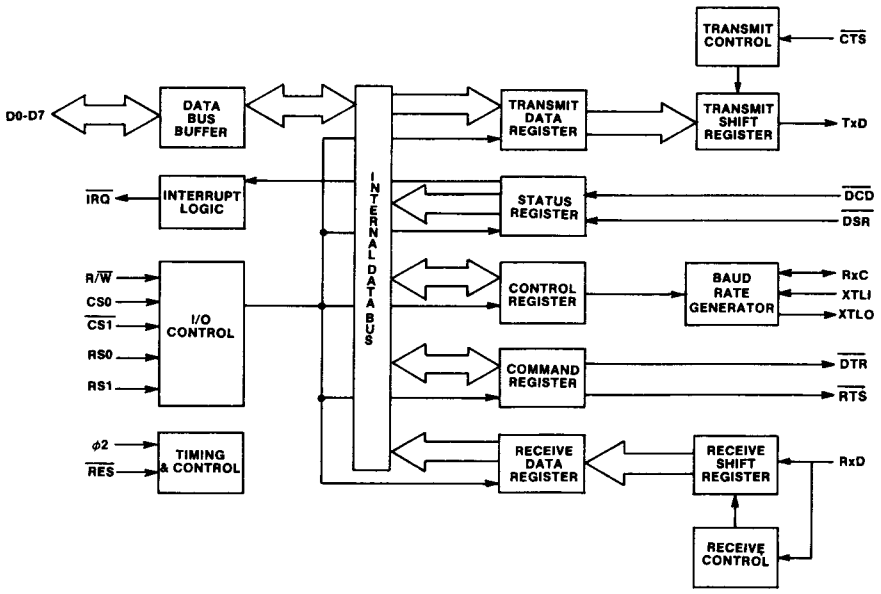


Fig. 2 - Internal organization. 92CM-36890RI

TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus and the registers, the Data Bus Buffer, and the microprocessor data bus, and the hardware reset features.

Timing is controlled by the system $\phi 2$ clock input. The chip will perform data transfers to or from the microcomputer data bus during the $\phi 2$ high period when selected.

All registers will be initialized by the Timing and Control Logic when the Reset ($\overline{RES}$) line goes low. See the individual register description for the state of the registers following a hardware reset.

TRANSMITTER AND RECEIVER DATA REGISTERS

These registers are used a temporary data storage for the CDP65C51/51A Transmit and Receive circuits. Both the mitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Data Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are "don't care".

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are "0". Parity bits are not contained in the Receiver Data Register. They are stripped off after being used for parity checking.

STATUS REGISTER

Fig. 3 indicates the format of the CDP65C51/51A Status Register. A description of each status bit follows.

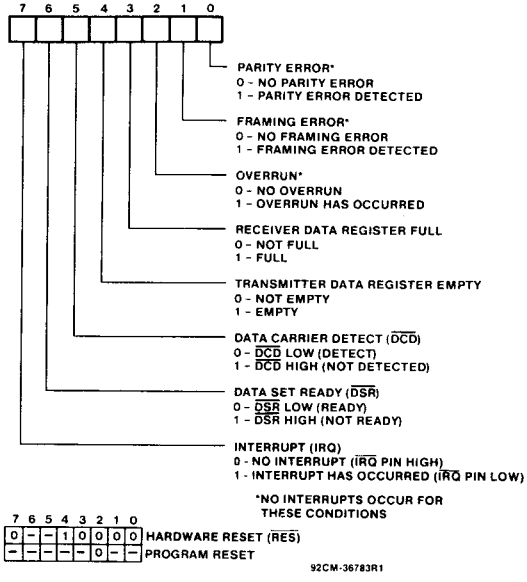


Fig. 3 - Status register format.

Receiver Data Register Full (Bit 3)

This bit goes to a "1" when the CDP65C51/51A transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a "0" when the processor reads the Receiver Data Register.

Transmitter Data Register Empty (Bit 4)

This bit goes to a "1" when the CDP65C51/51A transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a "0" when the processor writes new data onto the Transmitter Data Register.

Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the $\overline{DCD}$ and $\overline{DSR}$ inputs to the CDP65C51/51A. A "0" indicates a high (false). Whenever either of these inputs changes state, an immediate processor interrupt occurs, unless the CDP65C51/51A is disabled (bit 0 of the Command Register is a "0"). When the interrupt occurs, the status bits will indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until the Status Register is interrogated by the processor. At that time, another interrupt will immediately occur and the status bits will reflect the new input levels.

Framing Error (Bit 1), Overrun (Bit 2), and Parity Error (Bit 0)

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified.

Interrupt (Bit 7)

This bit goes to a "0" when the Status Register has been read by the processor, and goes to a "1" whenever any kind of interrupt occurs.

CONTROL REGISTER

The Control Register selects the desired transmitter baud rate, receiver clock source, word length, and the number of stop bits.

Selected Baud Rate (Bits 0, 1, 2, 3)

These bits, set by the processor, select the Transmitter baud rate, which can be at 1/16 an external clock rate or one of 15 other rates controlled by the internal baud-rate generator as shown in Fig. 4.

Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A "0" causes the Receiver to operate at a baud rate of 1/16 an external clock. A "1" causes the Receiver to operate at the same baud rate as is selected for the transmitter as shown in Fig. 4.

Word Length (Bits 5, 6)

These bits determine the word length to be used (5, 6, 7 or 8 bits). Fig. 4 shows the configuration for each number of bits desired.

Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A "0" always indicates one stop bit. A "1" indicates 1½ stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, and 2 stop bits in all other configurations.

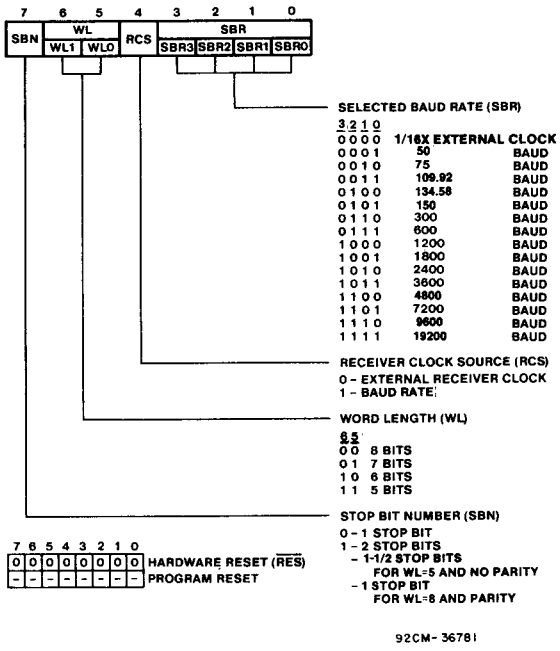
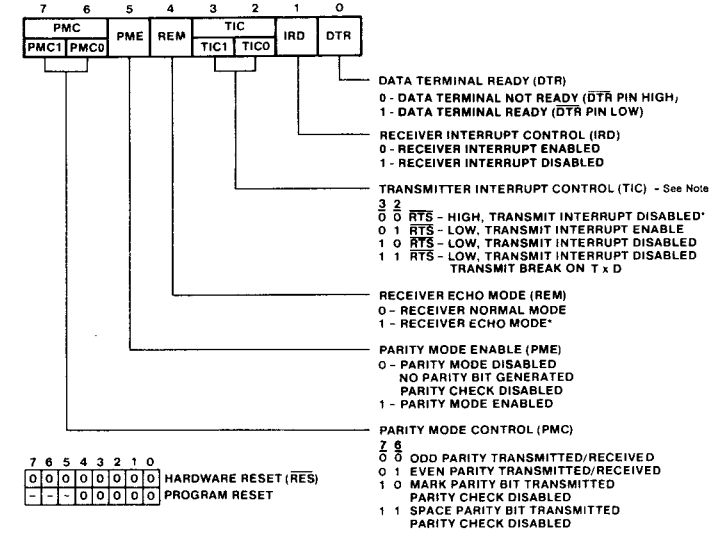


Fig. 4 - CDP65C51/51A control register.

COMMAND REGISTER

The Command Register controls specific modes and functions (Fig. 5).



*BITS 2 AND 3 MUST BE ZERO FOR RECEIVER ECHO MODE. RTS WILL BE LOW.

Fig. 5 - CDP65C51/51A command register 92CM-36790R1

Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready (DTR) line. A "0" indicates the microcomputer system is not ready by setting the DTR line high. A "1" indicates the microcomputer system is ready be setting the DTR line low. When the DTR bit is set to a "0", the receiver and transmitter are both disabled.

Receiver Interrupt Control (Bit 1)

This bit disables the Receiver from generating an interrupt when set to a "1". The Receiver interrupt is enabled when this bit is set to a "0" and Bit 0 is set to a "1".

Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send (RTS) line and the Transmitter interrupt. Fig. 5 shows the various configurations of the RTS line and Transmit Interrupt bit settings.

Receiver Echo Mode (Bit 4)

This bit enables the Receiver Echo Mode. Bits 2 and 3 must be zero. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by ½ bit time. A "1" enables the Receiver Echo Mode. A "0" bit disables the mode.

Parity Mode Enable (Bit 5)

This bit enables parity bit generation and checking. A "0" disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A "1" bit enables generation and checking of parity bits.

Parity Mode Control (Bits 6, 7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check). Fig. 5 shows the possible bit configurations for the Parity Mode Control bits.

NOTE: When changing command register bits 3 and 2 from 0,1 to 1,0 a 'break' may be generated. To avoid the generation of this break, always change from 0,1 to 0,0 to 1,0.

TRANSMITTER AND RECEIVER

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the transmitter, then RxC becomes an output and can be used to slave other circuits to the CDP65C51/51A. Fig. 6 shows the Transmitter and Receiver layout.

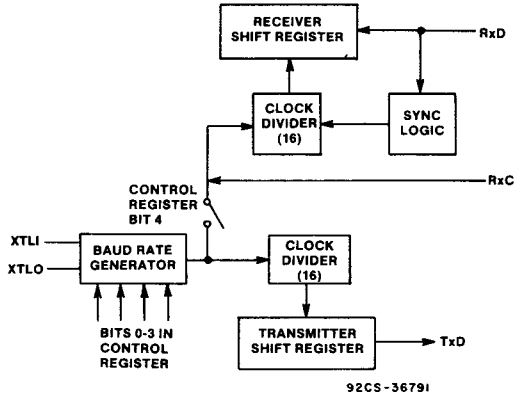


Fig. 6 - Transmitter receiver clock circuits.

CDP65C51/51A OPERATION

TRANSMITTER AND RECEIVER OPERATION

Continous Data Transmit (Fig. 7)

In the normal operating mode, the processor interrupt ($\overline{IRQ}$) is used to signal when the CDP65C51/51A is ready to accept the next data word to be transmitted. This interrupt occurs at the beginning of the Start Bit. When the processor reads the Status Register of the CDP65C51/51A, the interrupt is cleared. The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "Mark" will be transmitted.

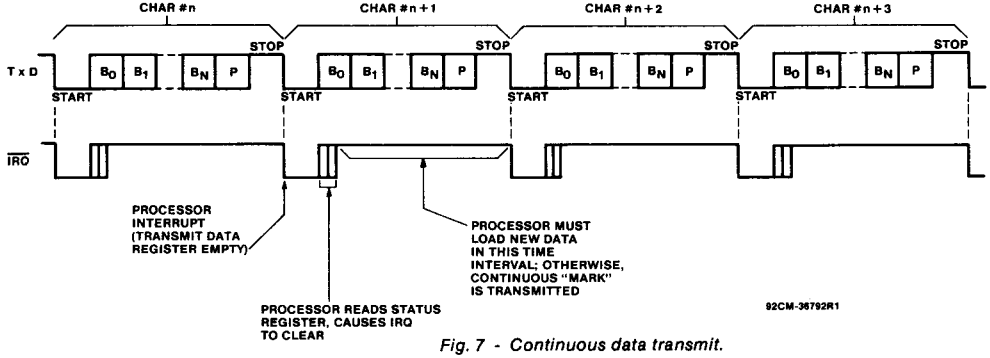


Fig. 7 - Continuous data transmit.

Similar to the above case, the normal mode is to generate a processor interrupt when the CDP65C51/51A has received a full data word. This occurs at about the 8/16 point through the Stop Bit. The processor must read the Status Register and rad the data word before the next interrupt, otherwise the Overrun condition occurs.

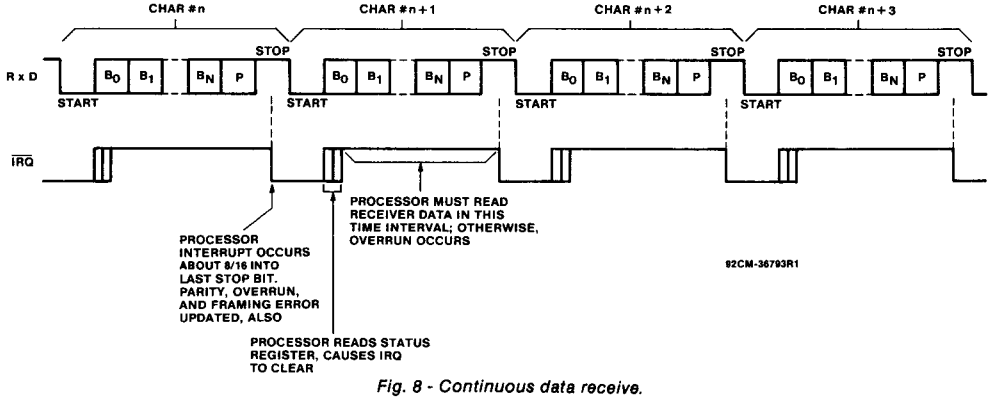


Fig. 8 - Continuous data receive.

Transmit Data Register Not Loaded By Processor (Fig. 9)

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line will go to the "MARK" condition until the data is loaded. When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word.

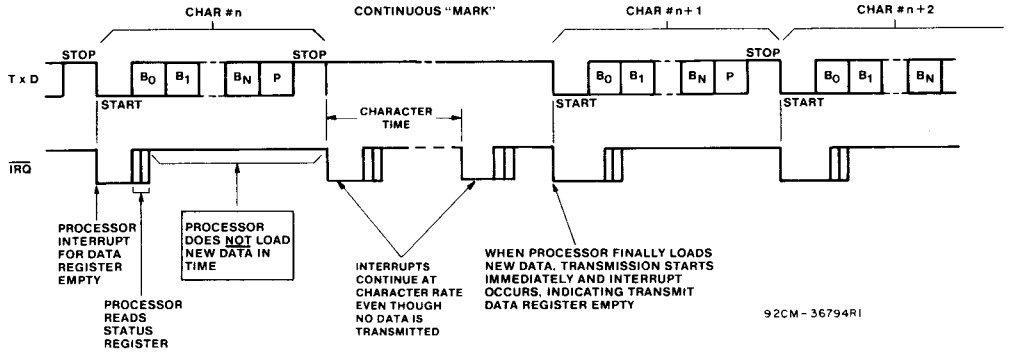


Fig. 9 - Transmit data register not loaded by processor.

Effect of $\overline{CTS}$ on CDP65C51 Transmitter (Fig. 10)

$\overline{CTS}$ is the Clear-to-Send signal generated by the modem. It is normally low (true state) but may go high in the event of some modem problems. When this occurs, the TxD line immediately goes to the "Mark" condition. Interrupts continue at the same rate, but the Status Register does not indicate the Transient Data Register is empty. Since there is no status bit for $\overline{CTS}$, the processor must deduce that $\overline{CTS}$ has gone to the False (high) state. This is covered later. $\overline{CTS}$ is a transmit control line only, and has no effect on the CDP65C51 Receiver Operation.

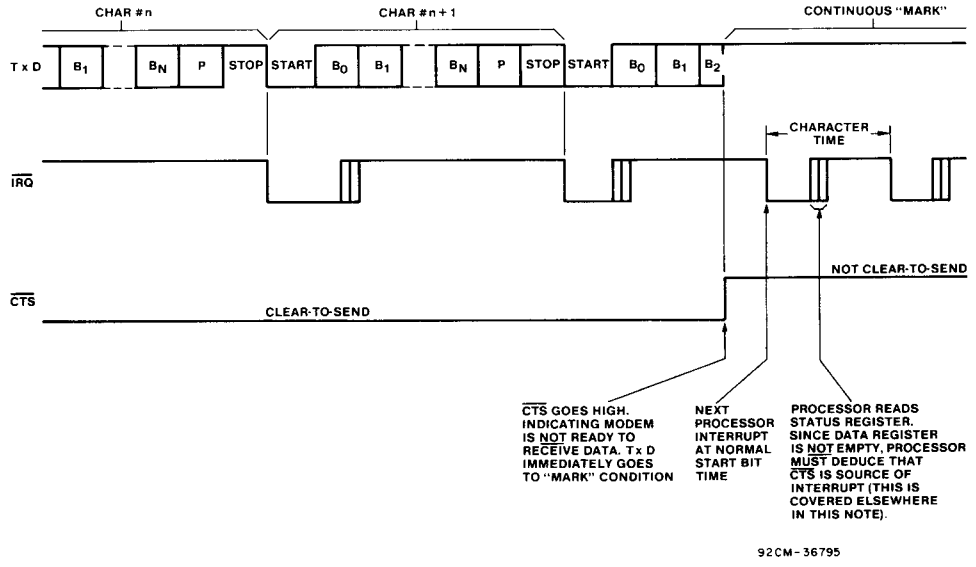


Fig. 10 - Effect of $\overline{CTS}$ on CDP65C51 transmitter

TRANSMITTER AND RECEIVER OPERATION (Cont'd)

Effect of $\overline{CTS}$ on CDP65C51A Transmitter (Fig. 10A)

$\overline{CTS}$ is the Clear-to-Send signal generated by the modem. It is normally low (true state) but may go high in the event of some modem problems. When this occurs, the TxD line goes to the "MARK" condition following the complete transmission of any character which is currently being shifted out of the Transmitter Shift Register. Since there is no status bit for $\overline{CTS}$, the processor must deduce that $\overline{CTS}$ has gone to the False (high) state. This is covered later. $\overline{CTS}$ is a transmit control line only, and has no effect on the CDP65C51A Receiver Operation. Normal transmission will resume when $\overline{CTS}$ goes low again.

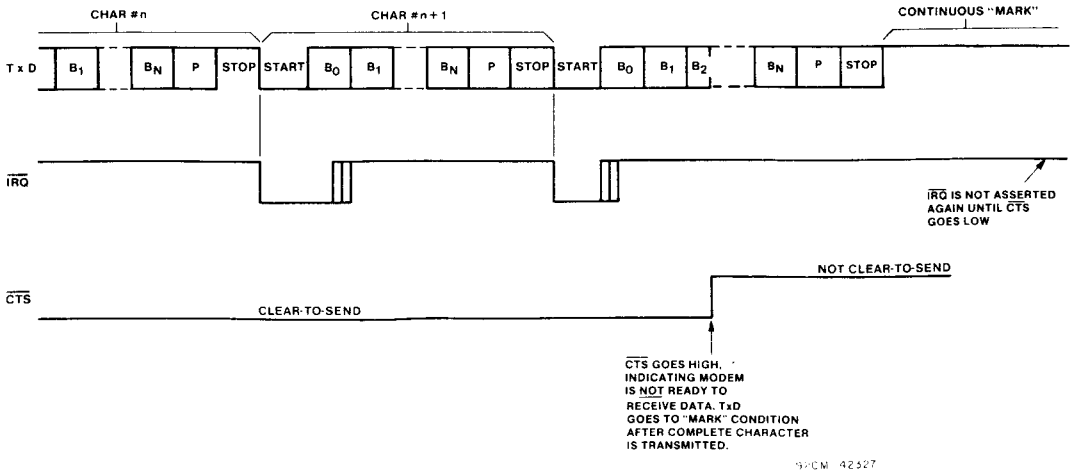


Fig. 10A - Effect of CTS on CDP65C51A transmitter

Effect of Overrun on Receiver (Fig. 11)

If the processor does not read the Receiver Data Register in the allocated time, then, when the following interrupt occurs, the new data word is not transferred to the Receiver Data Register, but the Overrun status bit is set. Thus, the Data Register will contain the last valid data word received and all following data is lost.

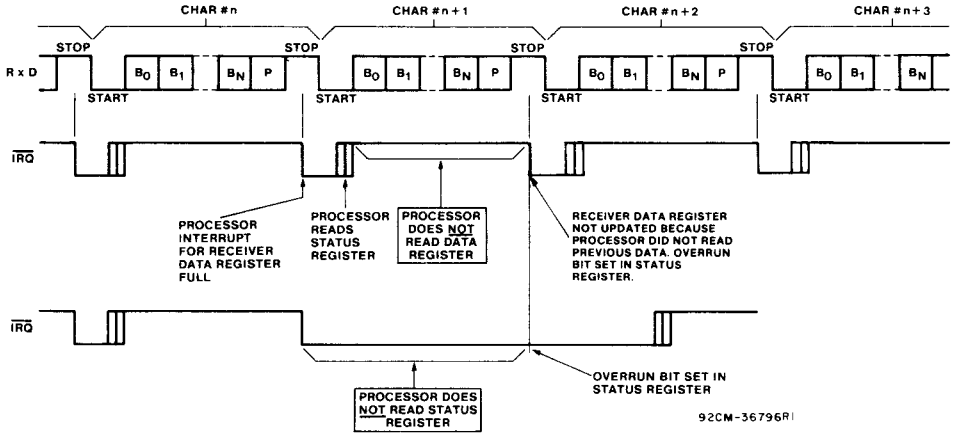


Fig. 11 - Effect of overrun on receiver.

TRANSMITTER AND RECEIVER OPERATION (Cont'd)

Echo Mode Timing (Fig. 12)

In Echo Mode, the TxD line re-transmits the data on the RxD line, delayed by ½ of the bit time.

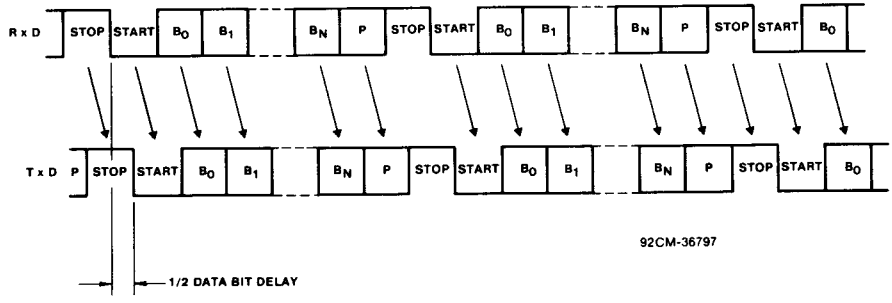


Fig. 12 - Echo mode timing.

Effect of $\overline{CTS}$ on Echo Mode Operation (Fig. 13)

See "Effect of $\overline{CTS}$ on Transmitter" for the effect of $\overline{CTS}$ on the Transmitter. Receiver operation is unaffected by $\overline{CTS}$, so, in Echo Mode, the Transmitter is affected in the same way as "Effect of $\overline{CTS}$ on Transmitter". In this case however, the processor interrupts signify that the Receiver Data Register is full, so the processor has no way of knowing that the Transmitter has ceased to echo.

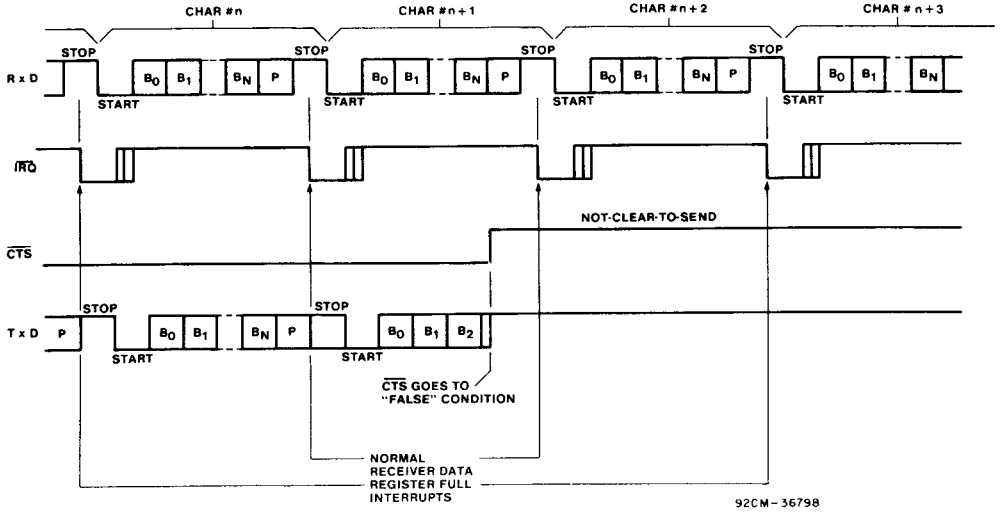


Fig. 13 - Effect of $\overline{CTS}$ on echo mode.

TRANSMITTER AND RECEIVER OPERATION (Cont'd)

Overrun in Echo Mode (Fig. 14)

If Overrun occurs in Echo Mode, the Receiver is affected the same way as described in "Effect of Overrun on Receiver".

For the re-transmitted data, when overrun occurs, the TxD line goes to the "MARK" condition until the first Start Bit after the Receiver Data Register is read by the processor.

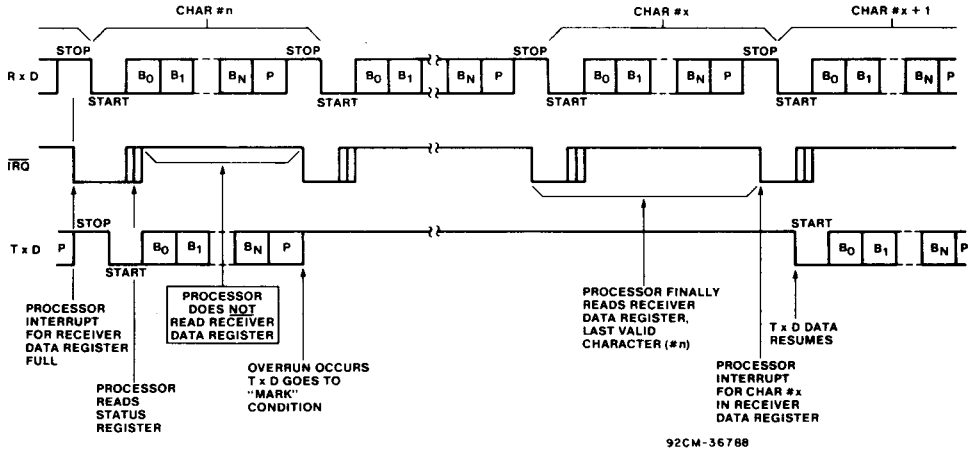


Fig. 14 - Overrun in echo mode.

Framing Error (Fig. 15)

Framing Error is caused by the absence of Stop Bit(s) on received data. The status bit is set when the processor interrupt occurs. Subsequent data words are tested for Framing Error separately, so the status bit will always reflect the last data word received.

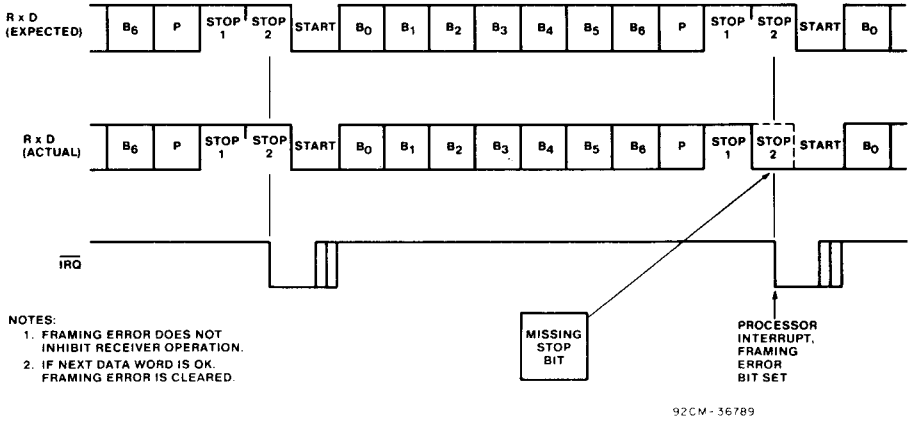


Fig. 15 - Framing error.

TRANSMITTER AND RECEIVER OPERATION (Cont'd)

Effect of $\overline{DCD}$ on Receiver (Fig. 16)

$\overline{DCD}$ is a modem output used to indicate the status of the carrier frequency detection circuit of the modem. This line goes high for a loss of carrier. Normally, when this occurs, the modem will stop transmitting data (RxD on the CDP65C51/51A some time later). The CDP65C51/51A will cause a processor interrupt whenever $\overline{DCD}$ changes state and will indicate this condition via the Status Register.

Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the Status Register is read by the processor, the CDP65C51/51A automatically checks the level of the $\overline{DCD}$ line, and if it has changed, another interrupt occurs.

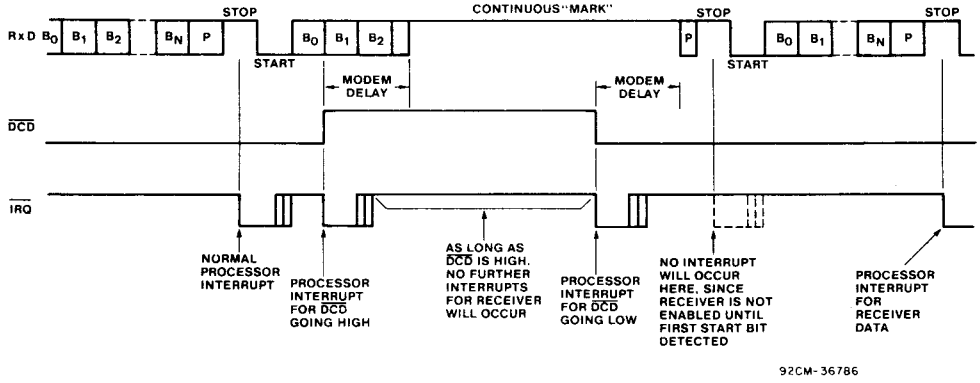


Fig. 16 - Effect of $\overline{DCD}$ on receiver.

Timing with 1½ Stop Bits (Fig. 17)

It is possible to select 1½ Stop Bits, but this occurs only for 5-bit data words with no parity bit. In this case, the processor interrupt for Receiver Data Register Full occurs halfway through the trailing half-Stop Bit.

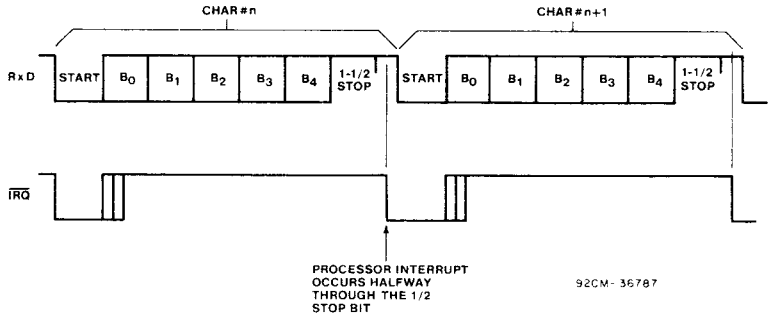


Fig. 17 - Timing with 1-1/2 stop bits.

TRANSMITTER AND RECEIVER OPERATION (Cont'd)

Transmit Continuous "BREAK" (Fig. 18)

The mode is selected via the CDP65C51/51A Command Register and causes the Transmitter to send continuous "BREAK" characters after both the transmitter and transmitter-holding registers have been emptied.

When the Command Register is programmed back to normal transmit mode, a Stop Bit is generated and normal transmission continues.

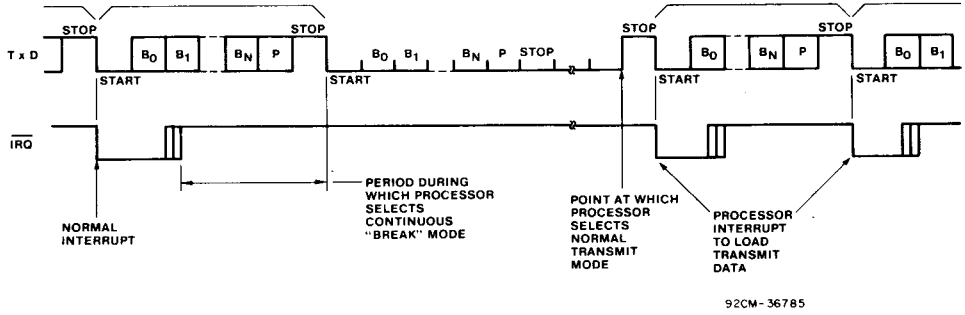


Fig. 18 - Transmit continuous "BREAK".

Receive Continuous "BREAK" (Fig. 19)

In the event the modem transmits continous "BREAK" characters, the CDP65C51/51A will terminate receiving.

Reception will resume only after a Stop Bit is encountered by the CDP65C51/51A.

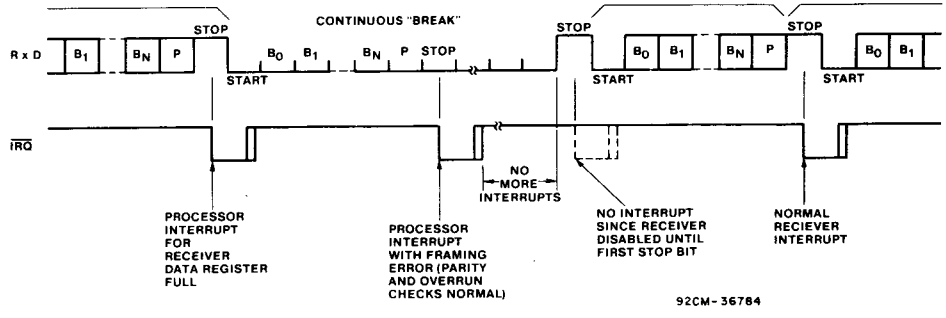


Fig. 19 - Receive continuous "BREAK".

STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the CDP65C51/51A should be interrogated, as follows:

1. Read Status Register

   This operation automatically clears Bit 7 (IRQ). Subsequent transitions on $\overline{DSR}$ and $\overline{DCD}$ will cause another interrupt.

2. Check IRQ Bit

   If not set, interrupt source is not the CDP65C51/51A.

3. Check $\overline{DCD}$ and $\overline{DSR}$

   These must be compared to their previous levels, which must have been saved by the processor. If they are both "0" (modem "on-line") and they are unchanged then the remaining bits must be checked.

4. Check RDRF (Bit 3)

   Check for Receiver Data Register Full.

5. Check Parity, Overrun, and Framing Error (Bits 0-2)

   Only if Receiver Data Register is Full.

6. Check TDRE (Bit 4)

   Check for Transmitter Data Register Empty.

7. If none of the above, then $\overline{CTS}$ must have gone to the False (high) state.

PROGRAMMED RESET OPERATION

A program reset occurs when the processor performs a write operation to the CDP65C51/51A with RS0 high and RS1 low. The program reset operates somewhat different from the hardware reset ($\overline{RES}$ pin) and is described as follows:

1. Internal registers are not completely cleared. The data sheet indicates the effect of a program reset on internal registers.
2. The $\overline{DTR}$ line goes high immediately.
3. Receiver and transmitter interrupts are disabled immediately. If $\overline{IRQ}$ is low when the reset occurs, it stays low until serviced, unless interrupt was caused by $\overline{DCD}$ or $\overline{DSR}$ transition.
4. $\overline{DCD}$ and $\overline{DSR}$ interrupts disabled immediately. If $\overline{IRQ}$ is low and was caused by $\overline{DCD}$ or $\overline{DSR}$, then it goes high, also $\overline{DCD}$ and $\overline{DSR}$ status bits subsequently will follow the input lines, although no interrupt will occur.
5. Overrun cleared, if set.

MISCELLANEOUS NOTES ON OPERATION

1. If Echo Mode is selected, $\overline{RTS}$ goes low.
2. If Bit 0 of Command Register is "0" (disabled), then:
   a) All interrupts disabled, including those caused by $\overline{DCD}$ and $\overline{DSR}$ transitions.
   b) Receiver disabled, but a character currently being received will be completed first.
   c) Transmitter is disabled after both the Transmit Data and Transmit Shift Registers have been emptied.
3. Odd parity occurs when the sum of all the "1" bits in the data word (including the parity bit) is odd.
4. In the Receive Mode, the received parity bit does not go into the Receiver Data Register, but is used to generate parity error for the Status Register.
5. Transmitter and Receiver may be in full operation simultaneously. This is "full-duplex" mode.
6. If the RxD line inadvertently goes low and then high during the first 9 receiver clocks after a Stop Bit; a false Start Bit will result.

   For false Start Bit detection, the CDP65C51/51A does not begin to receive data, instead, only a true Start Bit initiates receiver operation.
7. A precaution to consider with the crystal oscillator circuit is:
   The XTLI input may be used as an external clock input. The XTLO pin must be floating and may not be used for any other function.
8. $\overline{DCD}$ and $\overline{DSR}$ transitions, although causing immediate processor interrupts, have no effect on transmitter operation. Data will continue to be sent, unless the processor forces transmitter to turn off. Since these are high-impedance inputs, they must not be permitted to float (un-connected). If unused, they must be terminated either to Gnd or V_{DD}.

GENERATION OF NON-STANDARD BAUD RATES

Divisors

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the CDP65C51/51A Control Register.

The divisors, then, are determined by bits 0-3 in the Control Register and their values are shown in Table II.

Generating Other Baud Rates

By using a different crystal, other baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the CDP65C51/51A with an off chip oscillator to achieve the same thing. In this case, XTLI (pin 6) must be the clock input and XTLO (pin 7) must be a no connect.

CDP65C51/51A OPERATION (Cont'd)

Table II - Divisor Selection

CONTROL REGISTER BITS				DIVISOR SELECTED FOR THE INTERNAL COUNTER	BAUD RATE GENERATED WITH 1.8432 MHz	BAUD RATE GENERATED WITH FREQUENCY (F)
3	2	1	0			
0	0	0	0	No Divisor Selected	1/16 of External Clock at Pin XTLI	1/16 of External Clock at Pin XTLI
0	0	0	1	36,864	$\frac{1.8432 \times 10^6}{36,864} = 50$	$\frac{F}{36,864}$
0	0	1	0	24,576	$\frac{1.8432 \times 10^6}{24,576} = 75$	$\frac{F}{24,576}$
0	0	1	1	16,768	$\frac{1.8432 \times 10^6}{16,768} = 109.92$	$\frac{F}{16,768}$
0	1	0	0	13,696	$\frac{1.8432 \times 10^6}{13,696} = 134.58$	$\frac{F}{13,696}$
0	1	0	1	12,288	$\frac{1.8432 \times 10^6}{12,288} = 150$	$\frac{F}{12,288}$
0	1	1	0	6,144	$\frac{1.8432 \times 10^6}{6,144} = 300$	$\frac{F}{6,144}$
0	1	1	1	3,072	$\frac{1.8432 \times 10^6}{3,072} = 600$	$\frac{F}{3,072}$
1	0	0	0	1,536	$\frac{1.8432 \times 10^6}{1,536} = 1200$	$\frac{F}{1,536}$
1	0	0	1	1,024	$\frac{1.8432 \times 10^6}{1,024} = 1800$	$\frac{F}{1,024}$
1	0	1	0	768	$\frac{1.8432 \times 10^6}{768} = 2400$	$\frac{F}{768}$
1	0	1	1	512	$\frac{1.8432 \times 10^6}{512} = 3600$	$\frac{F}{512}$
1	1	0	0	384	$\frac{1.8432 \times 10^6}{384} = 4800$	$\frac{F}{384}$
1	1	0	1	256	$\frac{1.8432 \times 10^6}{256} = 7200$	$\frac{F}{256}$
1	1	1	0	192	$\frac{1.8432 \times 10^6}{192} = 9600$	$\frac{F}{192}$
1	1	1	1	96	$\frac{1.8432 \times 10^6}{96} = 19200$	$\frac{F}{96}$

DIAGNOSTIC LOOP-BACK OPERATING MODES

A simplified block diagram for a system incorporating a CDP65C51/51A is shown in Fig. 20.

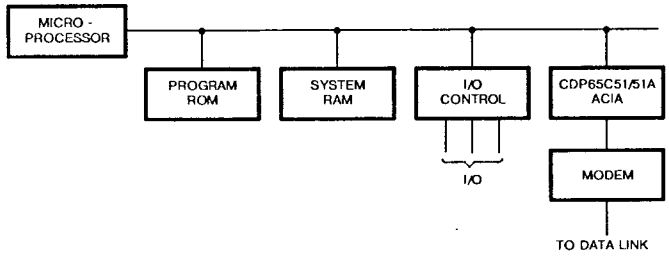


Fig. 20 - Simplified system diagram.

DIAGNOSTIC LOOP-BACK OPERATING MODES (Cont'd)

Occasionally it may be desirable to include in the system a facility for "loop-back" diagnostic testing, of which there are two kinds:

1. Local Loop-Back

   Loop-back from the point of view of the processor. In this case, the Modem and Data Link must be effectively disconnected and the ACIA transmitter connected back to its own receiver, so that the processor can perform diagnostic checks on the system, excluding the actual data channel.

2. Remote Loop-Back

   Loop-back from the point of view of the Data Link and Modem. In this case, the processor, itself, is disconnected and all received data is immediately retransmitted, so the system on the other end of the Data Link may operate independent of the local system.

The CDP65C51/51A does not contain automatic loop back operating modes, but they may be implemented with the addition of a small amount of external circuitry.

Fig. 21 indicates the necessary logic to be used with the CDP65C51/51A.

The LLB line is the positive-true signal to enable local loop-back operation. Essentially, LLB = high does the following:

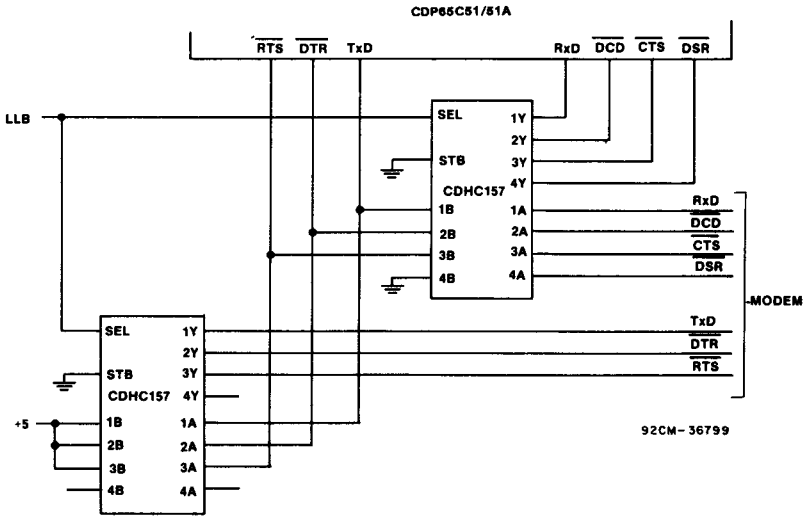
1. Disables outputs TxD, $\overline{DTR}$, and $\overline{RTS}$ (to Modem).
2. Disables inputs RxD, $\overline{DCD}$, $\overline{CTS}$, $\overline{DSR}$ (from Modem).
3. Connects transmitter outputs to respective receiver inputs:
   a) TxD to RxD
   b) $\overline{DTR}$ to $\overline{DCD}$
   c) $\overline{RTS}$ to $\overline{CTS}$

LLB may be tied to a peripheral control pin to provide processor control of local loop-back operation. In this way, the processor can easily perform local loop-back diagnostic testing.

Remote loop-back does not require this circuitry, so LLB must be set low. However, the processor must select the following:

1. Control Register bit 4 must be "1", so that the transmitter clock = receiver clock.
2. Command Register bit 4 must be "1" to select Echo Mode.
3. Command Register bits 3 and 2 must be "1" and "0", respectively, to disable transmitter interrupts.
4. Command Register bit 1 must be "0" to disable receiver interrupts.

In this way, the system retransmits received data without any effect on the local system.



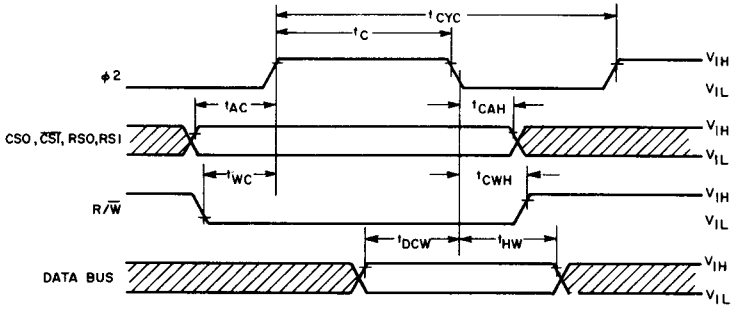
NOTES: 1. HIGH ON LLB SELECTS LOCAL LOOP-BACK MODE.
2. HIGH ON HC157 SELECT INPUT GATES "B" INPUTS TO "Y" OUTPUTS; LOW GATES "A" TO "Y".

Fig. 21 - Loop-back circuit schematic.

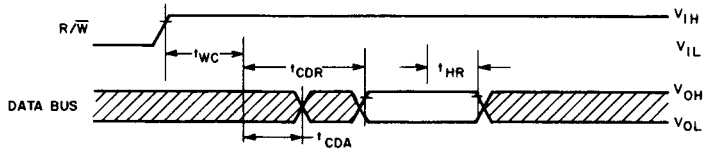
DYNAMIC ELECTRICAL CHARACTERISTICS—READ/WRITE CYCLE

V_{DD} = 5V ± 5%, T_A = -40°C to +85°C, C_L = 75pF

CHARACTERISTIC		LIMITS						UNITS
		CDP65C51-1 CDP65C51A-1		CDP65C51-2 CDP65C51A-2		CDP65C51-4 CDP65C51A-4		
		MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t_{CYC}	1	-	0.5	-	0.25	-	µs
φ2 Pulse Width	t_C	400	-	200	-	100	-	ns
Address Setup Time	t_{AC}	120	-	60	-	30	-	ns
Address Hold Time	t_{CAH}	0	-	0	-	0	-	ns
R/$\overline{W}$ Setup Time	t_{WC}	120	-	60	-	30	-	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	-	0	-	0	-	ns
Data Bus Setup Time	t_{DCW}	120	-	60	-	35	-	ns
Data Bus Hold Time	t_{HW}	20	-	10	-	5	-	ns
Read Access Time (Valid Data)	t_{CDR}	-	200	-	150	-	50	ns
Read Hold Time	t_{HR}	20	-	10	-	10	-	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	-	20	-	10	-	ns



Write-timing waveforms



Read-timing waveforms

92CM-36775

Fig. 22 - Timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS-TRANSMIT/RECEIVE, See Figs. 23, 24 and 25.
V_{DD} = 5V ±5%, T_A = -40°C to +85°C

CHARACTERISTIC		LIMITS						UNIT
		CDP65C51/51A-1		CDP65C51/51A-2		CDP65C51/51A-4		
		MIN	MAX	MIN	MAX	MIN	MAX	
Transmit/Receive Clock Rate	t_{CCY}	400*	-	325	-	250	-	ns
Transmit/Receive Clock High Time	t_{CH}	175	-	145	-	110	-	ns
Transmit/Receive Clock Low Time	t_{CL}	175	-	145	-	110	-	ns
XTLI to TxD Propagation Delay	t_{DD}	-	500	-	410	-	315	ns
RTS Propagation Delay	t_{DLY}	-	500	-	410	-	315	ns
IRQ Propagation Delay (Clear)	t_{IRQ}	-	500	-	410	-	315	ns
RES Pulse Width	t_{RES}	400	-	300	-	200	-	ns

(t_r, t_f = 10ns to 30ns)

* The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

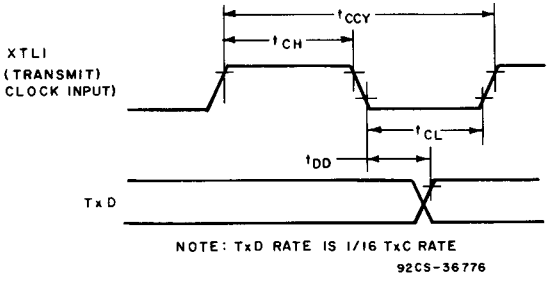


Fig. 23 - Transmit timing waveforms with external clock.

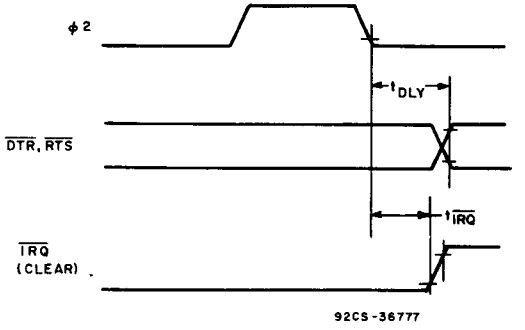


Fig. 24 - Interrupt and output timing waveforms.

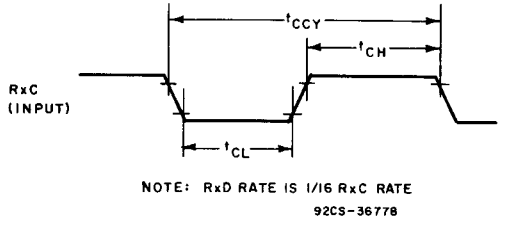


Fig. 25 - Receive external clock timing waveforms.

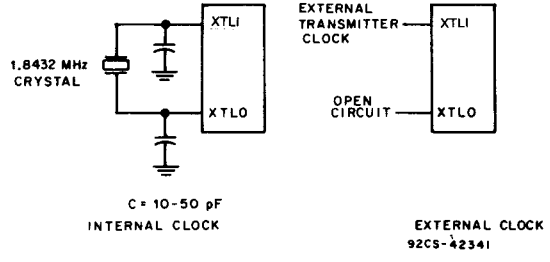


Fig. 26 - Transmitter clock generation.